

L1: Entry 7 of 9

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TITLE: High performance cpd. semiconductor device - includes
interface of metal semiconductor insulator semiconductor,
semiconductor-semiconductor with sulphur layer NoAbstract Dwg 1a/2

PRIORITY-DATA: 1990JP-0058062 (March 12, 1990), 1990JP-0058062
(March 12, 1990)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP <u>03261147</u> A	November 21, 1991		000	

INT-CL (IPC): H01L 21/33; H01L 29/81

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SEMICONDUCTOR DEVICE, AND METHOD AND APPARATUS FOR MANUFACTURING SEMICONDUCTOR DEVICE

Publication Number: 03-261147 (JP 3261147 A) , November 21, 1991

Inventors:

- SUGAWARA HIROHIKO
- OSHIMA MASA HARU

Applicants

- NIPPON TELEGR & TELEPH CORP (A Japanese Company or Corporation), JP (Japan)

Application Number: 02-058062 (JP 9058062) , March 12, 1990

International Class (IPC Edition 5):

- H01L-021/338
- H01L-021/203
- H01L-029/812

JAPIO Class:

- 42.2 (ELECTRONICS--- Solid State Components)

JAPIO Keywords:

- R002 (LASERS)
- R020 (VACUUM TECHNIQUES)
- R095 (ELECTRONIC MATERIALS--- Semiconductor Mixed Crystals)
- R097 (ELECTRONIC MATERIALS--- Metal Oxide Semiconductors, MOS)

Abstract:

PURPOSE: To increase the degree of freedom in design and improve device quality by forming a sulfur or selenium layer before forming metal. insulator, and semiconductor layers.

CONSTITUTION: In a compound semiconductor device, a sulfur or selenium layer 3 is formed between metal layers 4-6 and a semiconductor layer 2, or between an insulating layer 7 and semiconductor layers 2 and 1, or between semiconductor layers 2 and 1. According to this structure, a stabilized clean surface is obtained while eliminating adverse effects of spontaneous oxidation, and it is possible to realize a barrier height that depends greatly on the work function of metal. Therefore, the degree of freedom in design is increased, and thus a high-quality device can be obtained easily. (From: *Patent Abstracts of Japan*, Section: E, Section No. 1168, Vol. 16, No. 67, Pg. 21, February 19, 1992)

JAPIO

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High performance cpd. semiconductor device - includes interface of metal semiconductor insulator semiconductor, semiconductor-semiconductor with sulphur layer NoAbstract Dwg 1a/2
Patent Assignee: NIPPON TELEGRAPH & TELEPHONE CORP

Patent Family

Patent Number	Kind	Date	Application Number	Kind	Date	Week	Type
JP 3261147	A	19911121	JP 9058062	A	19900312	199202	B

Priority Applications (Number Kind Date): JP 9058062 A (19900312); JP 9058062 A (19900312)

Derwent World Patents Index

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Dialog® File Number 351 Accession Number 8884551

******* Dialog**

Basic Patent (Number,Kind,Date): JP 9330982 A2 19971222

PATENT FAMILY:

Japan (JP)

Patent (Number,Kind,Date): JP 9330982 A2 19971222

FORMATION OF INTERLAYER INSULATING FILM OF SEMICONDUCTOR DEVICE
(English)

Patent Assignee: SAM SUNG ELECTRONIC

Author (Inventor): SAI SHIGEN; RI KAITEI; KOU HEIKIN; GU SHIYUZEN

Priority (Number,Kind,Date): KR 969578 A 19960330

Applic (Number,Kind,Date): JP 9758062 A 19970312

IPC: * H01L-021/768; H01L-021/316

CA Abstract No: ; 128(07)083174V

Derwent WPI Acc No: ; G 98-365504

Language of Document: Japanese

Korea, Republic (KR)

Patent (Number,Kind,Date): KR 255659 B1 20000501

METHOD OF APPLICATION SOG OF SEMICONDUCTOR DEVICE (English)

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (KR)

Author (Inventor): CHOI JI HYON (KR); LEE HAI JONG (KR); HOANG BYONG KUN (KR);
KU JU SONN (KR)

Priority (Number,Kind,Date): KR 969578 A 19960330

Applic (Number,Kind,Date): KR 969578 A 19960330

IPC: * H01L-021/31

CA Abstract No: * 128(07)083174V

Derwent WPI Acc No: * G 98-365504

Language of Document: Korean

United States of America (US)

Patent (Number,Kind,Date): US 5866476 A 19990202

METHODS FOR FORMING MOISTURE BLOCKING LAYERS (English)

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (KR)

Author (Inventor): CHOI JI-HYUN (KR); LEE HAE-JEONG (KR); HWANG BYUNG-
KEUN (KR); GOU JU-SON (KR)

Priority (Number,Kind,Date): KR 969578 A 19960330

Applic (Number,Kind,Date): US 826483 A 19970327

National Class: * 438624000; 433763000

IPC: * H01L-021/316

CA Abstract No: * 128(07)083174V

Derwent WPI Acc No: * G 98-365504

Language of Document: English

United States of America (US) - Legal Status

Number	Type	Date	Code	Text	
US 5866476	P	19960330	US AA	PRIORITY (PATENT)	
				KR 969578 A 19960330	
US 5866476	P	19970327	US AE	APPLICATION DATA (PATENT)	(APPL. DATA (PATENT))
				US 826483 A 19970327	
US 5866476	P	19970915	US AS02	ASSIGNMENT OF ASSIGNOR'S INTEREST	
				SAMSUNG ELECTRONICS CO., LTD. 416 MAETAN-DONG, PALDAL-GU SUWON-CITY, KYUNGKI-DO, ; CHOI, JI-HYUN : 19970410; LEE, HAE-JEONG : 19970410; HWANG, BYUNG- KEUN : 19970410; GOU, JU-SON : 19970410	
US 5866476	P	19990202	US A	PATENT	

INPADOC/Family and Legal Status

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Basic Patent (Number,Kind,Date): JP 3261147 A2 911121

PATENT FAMILY:

Japan (JP)

Patent (Number,Kind,Date): JP 3261147 A2 911121

SEMICONDUCTOR DEVICE, AND METHOD AND APPARATUS FOR MANUFACTURING
SEMICONDUCTOR DEVICE (English)

Patent Assignee: NIPPON TELEGRAPH & TELEPHONE

Author (Inventor): SUGAWARA HIROHIKO; OSHIMA MASAHARU

Priority (Number,Kind,Date): JP 9058062 A 900312

Applic (Number,Kind,Date): JP 9058062 A 900312

IPC: * H01L-021/338; H01L-021/203; H01L-029/812

CA Abstract No: ; 116(14)141967W

Derwent WPI Acc No: ; C 92-011820

JAPIO Reference No: ; 160067E000021

Language of Document: Japanese

INPADOC/Family and Legal Status

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